1. An inductive element comprising:

a semiconductor substrate having at least one semiconductor wall, said semiconductor wall including a top surface;

an insulating layer provided on said top surface; and

a conductive element located over said insulating layer, said conductive element being supported by said semiconductor wall.

2. The inductive element of claim 1, wherein said semiconductor wall includes silicon.

3. The inductive element of claim 1, wherein said substrate includes a cavity, and wherein said semiconductor wall is formed in said cavity.

4. The inductive element of claim 3, wherein said semiconductor wall has a height of about 200 microns.

5. The inductive element of claim 1, wherein said insulating layer includes an oxide.

6. The inductive element of claim 5, wherein said insulating layer includes silicon oxide.

7. The inductive element of claim 5, wherein said insulating layer has a thickness of about 100 Angstroms to about 500 Angstroms.

8. The inductive element of claim 1, further comprising a material formed between said at least one semiconductor wall and said semiconductor substrate.

9. The inductive element of claim 8, wherein said material includes resist.

10. The inductive element of claim 1, wherein said conductive element includes an electrically conductive material selected from the group consisting of metals and metal alloys.

11. The inductive element of claim 10, wherein said electrically conductive material is selected from the group consisting of copper, gold, tungsten and aluminum.

12. The inductive element of claim 10, wherein said electrically conductive material includes copper.

13. The inductive element of claim 1, wherein said conductive element includes at least one loop.

14. The inductive element of claim 13, wherein said loop has a thickness of about 0.3 microns to about 0.5 microns.

15. The inductive element of claim 13, wherein said loop includes copper.

16. The inductive element of claim 13, wherein said loop has a spiral configuration.

17. The inductive element of claim 1 further comprising a barrier layer over said insulating layer.

18. The inductive element of claim 17, wherein said barrier layer is formed of a material selected from the group consisting of titanium, titanium nitride, titanium tungsten, titanium nitride and chromium.

19. The inductive element of claim 17, wherein said barrier layer includes titanium nitride.

20. The inductive element of claim 1 further comprising a top insulating layer over said conductive element.

21. The inductive element of claim 1, wherein said semiconductor substrate has a plurality of semiconductor walls.

22. The inductive element of claim 21, wherein said substrate has a center portion, and said semiconductor walls extend radially from said center portion.

23. The inductive element of claim 1, wherein said semiconductor substrate is a silicon substrate.

24. The inductive element of claim 1, wherein said semiconductor substrate is a germanium substrate.

25. The inductive element of claim 1, wherein said semiconductor substrate is a gallium arsenide substrate.

26. A semiconductor device having a substrate and a cavity structure, a portion of said substrate being in contact with said cavity, said device comprising:

at least one semiconductor support element provided in said cavity, said semiconductor support element including a top surface;

an insulating layer provided on said top surface; and

a conductive element formed over said insulating layer, said conductive element being supported by said semiconductor support element.

27. The semiconductor substrate of claim 26, wherein said semiconductor support element has a height of about 200 microns.

28. The device of claim 26, wherein said semiconductor support element forms an angle with said conductive element.

29. The device of claim 26, wherein said angle is a 90° angle.

30. The device of claim 26, further comprising a resist material formed in said cavity structure, between said semiconductor support element and said substrate.

31. The device of claim 26, wherein said conductive element includes an electrically conductive material selected from the group consisting of metals and metal alloys.

32. The device of claim 31, wherein said electrically conductive material includes copper.

33. The device of claim 26, wherein said conductive element includes at least one loop.

34. The device of claim 33, wherein said loop has a thickness of about 0.3 microns to about 0.5 microns.

35. The device of claim 33, wherein said loop includes copper.

36. The device of claim 33, wherein said loop has a spiral configuration.

37. The device of claim 26 further comprising a barrier layer over said insulating layer.

38. The device of claim 37, wherein said barrier layer includes titanium nitride.

39. The device of claim 26 further comprising a top insulating layer over said conductive element.

40. The device of claim 26, wherein said semiconductor substrate has a plurality of semiconductor support elements formed in said cavity structure.

41. The device of claim 40, wherein said plurality of semiconductor support elements extends radially from a center portion of said cavity structure.

42. The device of claim 41, wherein said semiconductor support elements have a wall configuration.

43. The device of claim 41, wherein said semiconductor support elements have a column configuration.

44. A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, said integrated circuit including an inductive element, said inductive element comprising at least one semiconductor support with a top surface, said semiconductor support being formed in a cavity structure of a semiconductor substrate, said inductive element further comprising an insulating layer

provided over said top surface and a conductive element formed over said insulating layer and being supported by said semiconductor support.

45. The processor-based system of claim 44, wherein said semiconductor support includes silicon.

46. The processor-based system of claim 44, wherein said semiconductor support extends perpendicularly to said conductive element.

47. The processor-based system of claim 44, wherein said semiconductor support has a wall configuration.

48. The processor-based system of claim 44, wherein said conductive element is supported by portions of said semiconductor support.

49. The processor-based system of claim 46, wherein said semiconductor support has height of about 200 microns.

50. The processor-based system of claim 46, further comprising a material formed in said cavity structure, between said semiconductor support and said semiconductor substrate.

51. The processor-based system of claim 50, wherein said material includes resist.

52. The processor-based system of claim 46, wherein said conductive element includes an electrically conductive material selected from the group consisting of metals and metal alloys.

53. The processor-based system of claim 52, wherein said electrically conductive material is selected from the group consisting of copper, gold, tungsten and aluminum.

54. The processor-based system of claim 53, wherein said electrically conductive material includes copper.

55. The processor-based system of claim 46, wherein said conductive element includes at least one loop.

56. The processor-based system of claim 55, wherein said loop has a thickness of about 0.3 microns to about 0.5 microns.

57. The processor-based system of claim 55, wherein said loop includes copper.

58. The processor-based system of claim 55, wherein said loop has a spiral configuration.

59. The processor-based system of claim 46 further comprising a barrier layer over said insulating layer.

60. The processor-based system of claim 59, wherein said barrier layer includes a material selected from the group consisting of titanium, titanium nitride, titanium tungsten, titanium nitride and chromium.

61. The processor-based system of claim 46, wherein said semiconductor substrate has a plurality of semiconductor supports.

62. The processor-based system of claim 61, wherein said semiconductor supports extend radially from a center portion of said cavity structure.

63. The processor-based system of claim 44, wherein said semiconductor substrate is a silicon substrate..

64. The processor-based system of claim 44, wherein said semiconductor substrate is part of a memory circuit.

65. A method of forming an inductive element, said method comprising the steps of:

forming at least one semiconductor support element in a cavity structure, said at least one semiconductor support element having a top surface;

forming an insulating layer over said top surface; and

forming a conductive element over said insulating layer, said conductive element being supported by said semiconductor support element.

66. The method of claim 65, wherein said step of forming said semiconductor support element includes etching a semiconductor substrate.

67. The method of claim 66, wherein said step of etching said semiconductor substrate is achieved by using deep plasma etching.

68. The method of claim 68, wherein said at least one semiconductor support element is etched to about 200 microns.

69. The method of claim 65, wherein said step of forming said semiconductor support element further comprises forming a plurality of semiconductor walls which extend radially from a center portion of said cavity structure.

70. The method of claim 65 further comprising the step of forming said insulating layer of an oxide.

71. The method of claim 65 further comprising the step of locating a material in said cavity structure, between said semiconductor support element and said semiconductor substrate.

72. The method of claim 71, wherein said step of locating said material in said cavity structure is achieved by deposition.

73. The method of claim 71 further comprising the step of forming said material of resist.

74. The method of claim 65 further comprising the step of forming said conductive element of an electrically conductive material selected from the group consisting of metals and metal alloys.

75. The method of claim 74, wherein said electrically conductive material is selected from the group consisting of copper, gold, tungsten and aluminum.

76. The method of claim 75 wherein said electrically conductive material includes copper.

77. The method of claim 65, wherein said step of forming said conductive element further includes the step of forming at least one loop.

78. The method of claim 77, wherein said loop is formed to a thickness of about 0.3 microns to about 0.5 microns.

79. The method of claim 78, wherein said loop is formed of copper.

80. The method of claim 77, wherein said loop is formed in a spiral configuration.

81. The method of claim 65 further comprising the step of forming a barrier layer over said insulating layer.

82. The method of claim 81, wherein said barrier layer is formed of a material selected from the group consisting of titanium, titanium nitride, titanium tungsten, titanium nitride and chromium.

83. The method of claim 65 further comprising the step of forming a top insulating layer over said conductive element.